IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An integrated circuit comprising:

a peripheral interface to receive an interrupt request;

a memory interface to communicate with a memory device;

a processor interface to communicate with a processor; [[and]]

a logic circuit connected to the peripheral interface to acquire [[the]] an interrupt information associated with the interrupt request, wherein the logic circuit is also connected to the processor interface and the memory interface to pass the interrupt information to the memory device without passing the interrupt information to the processor interface ; and

a configuration circuit configured to store configuration address indicating a location in the memory device to store the interrupt information, wherein the configuration circuit is further configured to store configuration data indicating a number of devices the integrated circuit is configured to handle.

2. (Original) The integrated circuit of claim 1 further includes a memory unit to store the interrupt information before the interrupt information is passed to the memory interface.

3. (Currently Amended) The integrated circuit of claim 1 ~~further comprising a~~ , wherein the configuration circuit ~~to store configuration address indicating a location in the memory device to store the interrupt information~~ includes a read only memory device to store the configuration data.

4. (Currently Amended) The integrated circuit of claim 3, wherein the ~~configuration circuit includes a~~ read only memory device is also to store the configuration address.

5. (Original) The integrated circuit of claim 1 further comprising a graphics interface to communicate with a graphics card.

6. (Currently Amended) A system comprising:

a processor;

a memory device; and

a chipset connected to the processor and the memory device, wherein the chipset is configured to receive interrupt information and to pass the interrupt information to the memory device without notifying the processor the presence of the interrupt information, wherein the chipset includes an interrupt controller having a configuration circuit, wherein the configuration circuit is configured to store configuration address indicating a location in the memory device to store the interrupt information, and wherein the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle.

7. (Original) The system of claim 6, wherein the chipset includes a graphic and memory control hub to process graphic and memory information and to provide access between the processor and the memory device.

8. (Original) The system of claim 7, wherein the chipset further includes an input output control hub connected to the graphic and memory control hub to process input output information between the chipset and external devices.

9. (Currently Amended) The system of claim 8, wherein the ~~chipset further includes an~~ interrupt controller includes a logic circuit to receive the interrupt information, an interrupt circuit to store the interruption information, and a configuration circuit having a read only memory device to store the configuration address and the configuration data.

10. (Original) The system of claim 6, wherein the processor is configured to poll the memory device to check for the interrupt information at a time independent from a time the interrupt information is received by the chipset.

11. (Original) The system of claim 6 further comprising a second processor connected to the chipset.

12. (Original) The system of claim 11, wherein the second processor is configured to poll the memory device to check for the interrupt information at a time independent from a time the interrupt information is received by the chipset.

13. (Currently Amended) A method comprising:

receiving an interrupt request at an interrupt controller;

acquiring, at the interrupt controller, interrupt information corresponding to the interrupt request, wherein interrupt controller includes a configuration circuit, wherein the configuration circuit is configured to store configuration address indicating a location in the memory device to store the interrupt information, and wherein the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle; and

passing the interrupt information from the interrupt controller to a memory device without passing the interrupt information to a first processor.

14. (Currently Amended) The method of claim 13 further comprising:

polling the memory device to check for the interrupt information, wherein polling is performed by a second processor.

15. (Currently Amended) The method of claim 14, wherein polling is performed by the second processor at a time independent from a time the interrupt request is received by the interrupt controller.

16. (Currently Amended) The method of claim [[14]] 15 further comprising:

performing an interrupt function based on the interrupt information, wherein performing the interrupt function is carried out by the first processor.

17. (Currently Amended) The method of claim [[14]] 16, wherein ~~polling is performed by a second processor a time independent from a time the interrupt request is received by~~ the first processor and the second processor are connected to the interrupt controller through a single processor interface.

18. (Original) The method of claim 13, wherein the memory device and the interrupt controller are located in separate chips.

19. (Currently Amended) The method of claim 13, wherein passing the interrupt information from the interrupt controller to the memory device includes writing the interrupt information to the memory device at a memory location according [[to]] the configuration ~~information~~ address.

20. (Currently Amended) The method of claim 19, wherein the configuration ~~information~~ address is stored in a read only memory device of the interrupt controller.

21. (Currently Amended) A method comprising:

receiving an interrupt request at a chipset, the chipset connecting to a first processor;

acquiring, at the chipset, interrupt information corresponding to the interrupt request, wherein the chipset includes an interrupt controller having a configuration circuit, wherein the configuration circuit is configured to store configuration address indicating a location in the memory device to store the interrupt information, and wherein the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle;

storing the interrupt information at a memory location without notifying the first processor the interrupt request; and

polling the memory device to check for the interrupt information, wherein polling is performed at a time independent from a time the interrupt request is received at the chipset.

22. (Currently Amended) The method of claim 21, wherein polling is performed by the first processor.

23. (Original) The method of claim 21, wherein polling is performed by a second processor connected to the chipset.

24. (Currently Amended) The method of claim [[21]] 23 further comprising:

performing an interrupt function based on the interrupt information stored in the memory location, wherein performing the interrupt function is carried out by the first processor.

25. (Currently Amended) The method of claim 21, wherein storing the interrupt information at the memory location includes storing the interrupt information in a memory device separate from the first processor, the second processor, and the chipset.

26. (Currently Amended) The method of claim 25, wherein storing the interrupt information at the memory location includes storing the interrupt information at the memory location according to a configuration ~~information~~ address.

27. (Currently Amended) The method of claim 26, wherein the configuration information is stored in a random access memory device of the chipset.